What is claimed is:

1. A semiconductor memory device of a dynamic type for refreshing information stored in a memory space to hold the information continuously by amplifying the information stored in said memory space to rewrite the amplified information in said memory space, said memory device comprising:

a refresh control circuit for performing refreshment of the information only to a sub memory space which is in use when the refreshment of the information is performed, said sub memory space holding the information necessary to be refreshed, among a plurality of sub memory spaces formed by previous division of said memory space.

2. A semiconductor memory device of a dynamic type including a memory cell array for storing information, and a refresh circuit for refreshing the information stored in said memory cell array to hold the information continuously by amplifying the information stored in said memory cell array to rewrite the amplified information in said memory cell array, said memory device comprising:

a refresh control circuit for controlling an operation of said refresh circuit so as to perform refreshment of the information only to a sub memory space which is in use when the refreshment of the information is performed, said sub memory space holding the information necessary to be refreshed, among a plurality of sub memory spaces formed by previous division of an address space in a memory space of said memory cell array.

3. The semiconductor memory device according to

claim 2, wherein said refresh control circuit operates a logical product of data pertaining to whether each of said sub memory spaces are in use or not and refresh address data to be input to each address, and performs control of whether said refreshment is performed or not to each sub memory space with said refresh circuit on a basis of a result of said operation.

4. The semiconductor memory device according to claim 2, wherein a row decoder is added to said memory cell array, and said row decoder is set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and further said refresh control circuit is inserted between said memory cell array and said row decoder, said refresh control circuit set to intervene in a function of said row decoder for specifying the row address to which said refreshment is performed to control whether said refreshment is performed or not to each of said sub memory spaces.

5. The semiconductor memory device according to claim 2, wherein a row decoder is added to said memory cell array, and said row decoder is set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and further said refresh control circuit is provided in said row decoder, said refresh control circuit set to intervene in a function of said row decoder for specifying the row address to which said refreshment is performed to control whether the refreshment is performed or not to each of

said sub memory spaces.

6. The semiconductor memory device according to claim 2, wherein a row decoder and a refresh address counter are added to said memory cell array, and said row decoder and said refresh address counter are set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and further said refresh control circuit is attached to said refresh address counter, said refresh control circuit set to intervene in a function of said refresh address counter for outputting the row address to which said refreshment is performed to control whether the refreshment is performed or not to each of said sub memory spaces.

7. The semiconductor memory device according to claim 2, wherein a row decoder and a refresh address counter are added to said memory cell array, and said row decoder and said refresh address counter are set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and further said refresh control circuit is provided inside said refresh address counter, said refresh control circuit set to intervene in a function of said refresh address counter for outputting the row address to which said refreshment is performed to control whether the refreshment is performed or not to each of said sub memory spaces.

8. The semiconductor memory device according to

claim 2, wherein a row decoder, a multiplexer and a refresh address counter are connected to said memory cell array in this order, and said row decoder, said multiplexer and said refresh address counter are set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and further said refresh control circuit is inserted between said refresh address counter and said multiplexer, said refresh control circuit set to intervene in a refresh address counter's output of the row address to which said refreshment is performed, the output transmitted to said row decoder through said multiplexer, to control whether the refreshment is performed or not to each of said sub memory spaces.

9. The semiconductor memory device according to claim 2, wherein a row decoder, a multiplexer and a refresh address counter are connected to said memory cell array in this order, and said row decoder, said multiplexer and said refresh address counter are set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and further said refresh control circuit is provided inside said multiplexer, said refresh control circuit set to intervene in a refresh address counter's output of the row address to which said refreshment is performed, the output transmitted to said row decoder through said multiplexer, to control whether the refreshment is performed or not to each of said sub memory spaces.

10. The semiconductor memory device according to

claim 2, wherein said memory space is previously divided into different memory spaces to store different kinds of contents of information from one another, and at least one of said divided memory spaces are further divided into said plurality of sub memory spaces.

11. A refresh control circuit to be used for a semiconductor memory device of a dynamic type for refreshing information stored in a memory space to hold the information continuously by amplifying the information stored in said memory space to rewrite the amplified information in said memory space,

wherein said refresh control circuit performs control of refreshment of the information only to a sub memory space which is in use when the refreshment of the information is performed, said sub memory space holding the information necessary to be refreshed, among a plurality of sub memory spaces formed by previous division of said memory space.

12. A refresh control circuit to be used for a semiconductor memory device of a dynamic type including a memory cell array for storing information and a refresh circuit for refreshing the information stored in said memory cell array to hold the information continuously by amplifying the information stored in said memory cell array to rewrite the amplified information in said memory cell array,

wherein said refresh control circuit controls an operation of said refresh circuit so as to perform refreshment of the information only to a sub memory space

which is in use when the refreshment of the information is performed, said sub memory space holding the information necessary to be refreshed, among a plurality of sub memory spaces formed by previous division of an address space in a memory space of said memory cell array.

13. The refresh control circuit according to claim 12, wherein said refresh control circuit operates a logical product of data pertaining to whether each of said sub memory spaces are in use or not and refresh address data to be input to each address, and performs control of whether said refreshment is performed or not to each sub memory space with said refresh circuit on a basis of a result of said operation.

14. The refresh control circuit according to claim 12, wherein said memory space is previously divided into different memory spaces to store different kinds of contents of information from one another, and at least one of said divided memory spaces are further divided into said plurality of sub memory spaces.

15. A method for refreshing storage in a semiconductor memory device of a dynamic type for refreshing information stored in a memory space to hold the information continuously by amplifying the information stored in said memory space to rewrite the amplified information in said memory space, said method comprising the steps of:

dividing said memory space into a plurality of sub memory spaces in advance; and

performing refreshment of the information only to a sub memory space among the plurality of sub memory spaces, said sub memory space being in use when the refreshment of the information is performed, said sub memory space holding the information necessary to be refreshed.

16. A refresh method for refreshing information stored in a memory cell array to hold the information continuously by amplifying the information to rewrite the amplified information in said memory cell, said memory cell array is provided in a semiconductor memory device of a dynamic type, said method comprising the steps of:

dividing an address space in a memory space of said memory cell array into a plurality of sub memory spaces in advance; and

performing refreshment of the information only to a sub memory space among the plurality of sub memory spaces, said sub memory space being in use when the refreshment of the information is performed, said sub memory space holding the information necessary to be refreshed.

17. The refresh method according to claim 16, wherein a logical product of data pertaining to whether each of said sub memory spaces is in use or not and refresh address data to be input to each address is operated, and control of whether said refreshment is performed or not to each sub memory space is performed on a basis of a result of said operation.

18. The refresh method according to claim 16, wherein said memory space is previously divided into

different memory spaces to store different kinds of contents of information from one another, and at least one of said divided memory spaces is further divided into the plurality of sub memory spaces to perform control of said refreshment of the information to each of said sub memory spaces.